A 5.84 GHz Tunable SAW Oscillator with Frequency Doubler for a DSRC System

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Abstract — **A varactor tuned oscillator with an external SAW resonator and integrated frequency doubler is developed on a low cost 0.8 µm SiGe BiCMOS technology for a DSRC application. The measured phase noise is -95.5 dBc / Hz at 10 kHz offset on a single-ended 50 Ω load. A PMOS accumulation-mode varactor is used for the fine tuning of the oscillation frequency within a tuning range of 800 kHz. Furthermore a 2nd not tunable oscillator is fabricated with an improved phase noise of -105.65 dBc / Hz at 10 kHz offset. Frequency doubling is achieved by using two unbalanced emitter coupled pairs with a fundamental frequency rejection of better than 20 dBc.**

I. Introduction

Various wireless networks have been introduced during the last two decades and others are appearing such as DSRC (dedicated short-range communication). The 5.8 GHz-band active DSRC system used for ETC (electronic toll collection: automation collection of charges) in Japan is an infrastructure which forms the foundation for ITS (intelligent transport systems) [1]. The ITS comprises several standards, like WCDMA or WLAN in order to obtain a seamless communication in and around the vehicle. For full-scale implementation of ITS services, the DSRC system must be able to receive a large volume of information at high speed at a data rate up to 4 Mbps.
Due to this system constraints the performance on the RF front-end components are high. Particular, the spectral purity of the high frequencies generated in the front-end in order to convert the received frequency down to IF is a critical parameter in that system.

In section II the applied system concept has been discussed in contrast to alternative approaches, followed by a detailed description of the RF circuit blocks and the implementation. In section III the experience results are summarized and discussed with respect to the work in section II. Section IV gives a short conclusion on the achieved results.

II. Design Strategy

A. Architectural choice

Since SAW resonators are currently not available for operating frequencies higher than 3 GHz, a frequency multiplication is essential for SAW oscillator designs at 5.84 GHz. The common used techniques for frequency doubling is the amplification of the first harmonic while simultaneously suppressing the fundamental oscillator signal. This topology requires filters with high quality factors and basically much chip space for integrated inductors must be spent. Due to the needed passive components on chip the die size increases in contrast to the here proposed active frequency doubling techniques.

An active multiplication of the fundamental frequency with itself has been selected as the approach to circumvent the described problems. Fig. 1 shows the block level schematic of the oscillator system with a loop amplifier and an externally connected 2-port SAW resonator in its feedback path. Coplanar lines are used to interconnect the resonator with the amplifier in order to generate a proper phase shift without lossy components. The electric tunable circuit comprises an integrated varactor tuned phase shifter in the feedback path. This circuit operates as the fundamental wave oscillator and is buffered to drive the single-ended to differential converter.

A differential frequency doubler topology is required in order to obtain the needed fundamental frequency rejection in contrast to single-ended active doublers. The 50 Ω load resistance is directly applied to the output of the frequency doubler.

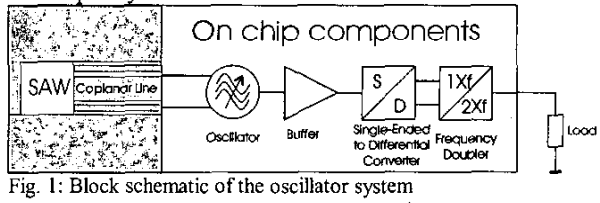

Fig. 1: Block schematic of the oscillator system

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B. Fundamental wave oscillator

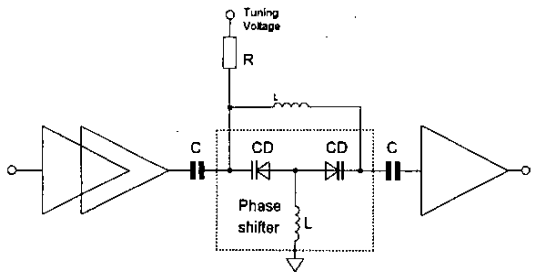

Fig. 2: Loop amplifier consisting of a tunable phase shifter

Fig. 2 shows the three stage loop amplifier with a phase shifter connected as a T-network between the 2nd and the 3rd stage. One integrated inductor is used with two accumulation mode PMOS transistors to obtain a tuning range of 40°. Another integrated inductor is connected to provide a dc path for the varactor and simultaneously blocking the RF path. This inductor could be replaced by a high resistor because of the neglecting current through the gate of the varactor. All amplifier stages are common emitter circuits with emitter degeneration because of the high input swing. The phase shift of each amplifier stage is about 190° at 2.92 GHz. The simulated overall phase shift of the loop amplifier with the phase shifter is between -100° and -140°.

A 2-port SAW resonator is used as the frequency determine device (Fig. 3) in the feedback path. Usually phase zero crossing occurs at this kind of SAW resonator at resonant frequency, but the static capacitances CT which arises due to the interdigitized metal fingers in the IDT's lead to a remaining phase shift of 40° at resonant

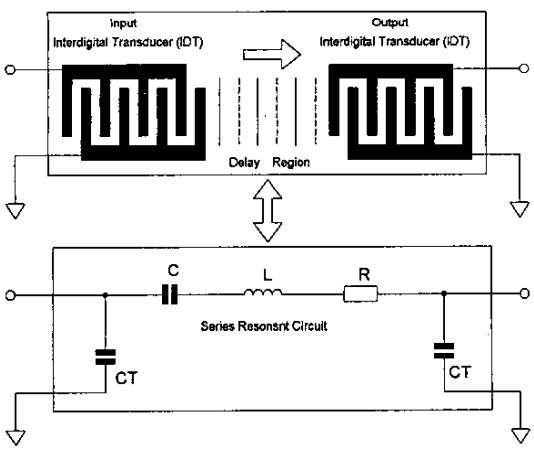

Fig.3: 2-port SAW resonator and the π equivalent circuit

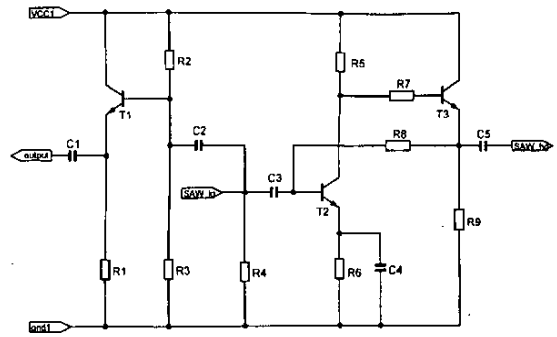

Fig. 4: Schematic of the loop amplifier with buffer stage for the 2nd oscillator chain without phase shifter

frequency. In order to eliminate the effect of the parasitic capacitors, chip inductors could be placed in parallel to the resonator ports. This helps to alter the phase shift, but a 3 dB higher insertion loss has been simulated for such a structure.

A 2nd not tunable loop amplifier was also investigated with the intention to minimize the phase noise. Frequency tuning is still possible by varying the length of the coplanar lines in the feedback path on the printed board. Fig. 4 shows the 2 stage shunt series feedback amplifier with T2, T3 and R8 as the resistive feedback. Additionally series emitter feedback is applied to T2. The advantage of the feedback paths is to obtain a possibility to adjust the input and output impedance in such a manner that optimal power transfer is possible [7][8]. Furthermore a high stability of the operating point is the result of a feedback amplifier. Even though some gain must be spent by using feedback techniques, the phase noise performance can be increased because of avoiding maximum gain current in the transistors which would increase transistor noise [9].

C. Single-ended to differential converter

An effective single-ended to differential converter regarding low power consumption and large signal compatibility is described in [5][6]. Such a class AB amplifier which amplifies the two half waves of the sinusoidal oscillator signal separately in two parallel braches (T1 and T2), is shown in Fig. 5. While one branch consisting of T1 can amplify the negative half wave of the input current in-phase, the other branch (T2) will primary amplify the positive half wave with inverted phase. The currents in the two branches are not linear, but as can be calculated by applying the translinear principle, the difference of the current is linear to the input signal, even for high signal levels [6].

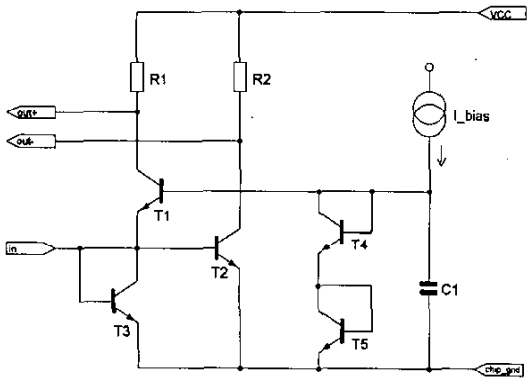

Fig. 5: Schematic of the single-ended to differential converter

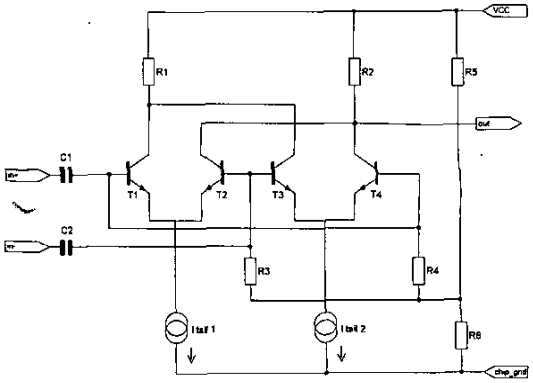

Fig. 6: Schematic of the frequency doubler

The input impedance is the parallel sum of the r_e's of T1 and T3 or T2 and T3 respectively, dependent on the sign of the input signal. Hence, the input impedance can be adjusted by varying the collector current because r_e of each transistor is V_T / I_C at this configuration.

Compared to a differential emitter coupled pair as a common single-ended to differential converter, the used circuit provides a higher linearity at large signals. Whereas several series connected emitter coupled pairs with emitter degeneration would be necessary to obtain the same linearity.

D. Frequency doubler

A gilbert cell mixer operating as a frequency doubler as well as a two unbalanced emitter coupled pair topology is compared regarding their circuit complexity. The gilbert cell mixer requires two input signals with the same frequency and a 90° phase difference. In order to save this 90° phase shifter, the two unbalanced emitter coupled pair topology, as shown in Fig. 6, is chosen.

This concept has a transfer function of a parabola for small input voltages when each emitter coupled pair consists of two transistors with different emitter area ratios n [4]. Because of this parabola transfer function the differential output current is expressed as a function of the square of the differential input voltage swing frequency. The best performance was achieved with a ratio of n=3. R1 and R2 transform this square current into a voltage swing. The simulated fundamental frequency rejection is more than 20 dB for this stage.

III. Experimental Results

A coplanar ceramic printed board was fabricated for the two versions of oscillators. The individual die was buried in a cavy in order to keep the wire bonds as short as possible. Coplanar lines with a characteristic wave impedance of 100 Ω are used to interconnect the SAW resonator with the loop amplifier. This is the same impedance than the remaining series resistance of the SAW resonator at its resonant frequency. Also the port impedances of the loop amplifier are about 100 Ω. Hence an optimal power transfer can be expected.

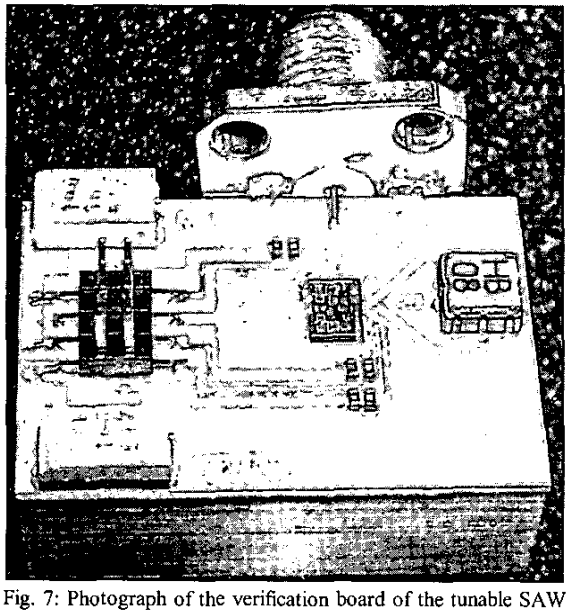

Fig. 7: Photograph of the verification board of the tunable SAW oscillator system

TABLE I
SUMMARY OF MEASUREMENT RESULTS

Parameter	Tunable Oscillator	Not Tunable Oscillator	Unit
Osc. freq.	5.8412 – 5.842	5.8416	GHz
Phase noise	- 95.5	-105.65	dBc / Hz @ 10 kHz
Max. Pout	- 23	- 21.3	dBm
Max. f_0 rejection	16	16	dBc
VCC	3 - 4	3 - 4	V
ICC	14.2	13.4	mA @ 3V

The length of these coplanar lines was chosen in that way, that the open loop phase is 0° at the oscillation frequency. Their calculated phase shift is 7.35° / mm. A 50 Ω coplanar line was used to connect the output of the oscillator chain with the SMA connector.

Fig. 8 shows the measured output signal of the oscillator system without tunable capability. A summary of the achieved measurement results are listed in Table I. Investigation on the fundamental frequency rejection shows a possibility to improve the achieved 16 dBc by increasing the output power of the fundamental wave oscillator and to minimize the ground inductance of the frequency doubler.

The phase noise of the fundamental frequency oscillator at 10 kHz was better than –105.65 dBc / Hz, since frequency multiplication of an oscillator signal results in increased SSB phase noise. A SSB phase noise of < -112 dBc / Hz at 10 kHz offset can be expected for the designed fundamental SAW oscillator [9]:

$$L(fm)_{Nf_0} = N^2 L(fm)_{f_0} + A \quad (1)$$

with N = multiplication factor
A = additive term

IV. CONCLUSION

A silicon integrated high performance SAW oscillator system has been successfully demonstrated which can be used in communication systems like DSRC without the need of using a complex synthesizer system to obtain the needed frequency stability. Even the center frequency of one SAW oscillator is adjustable over a wide frequency range. Although the performance of the SAW oscillator is very high, a low cost silicon 0.8µm SiGe BiCMOS process has been used. The low current consumption and the low supply voltage allows the use of these RF components in mobile applications.

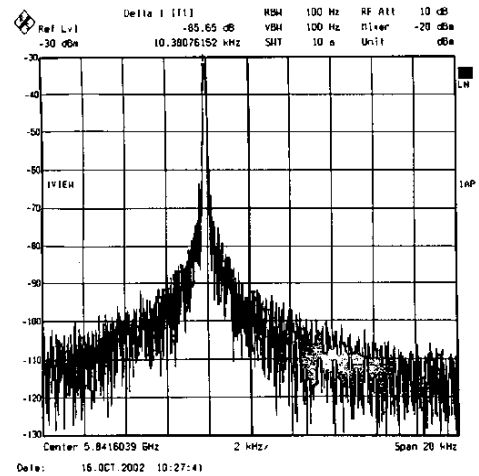

Fig. 8: Measured phase noise of the not tunable oscillator

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REFERENCES

[1] T. Omata, S. Ukai, M. Katagishi, S. Yoshida," Interactive wireless Communications for Wider-range ITS Services" *Hitachi review*, Vol. 49 (2000), No.3

[2] K. Kimura, "A bipolar four-quadrant-square multiplier consisting of unbalanced emitter-coupled pairs and expansions of its input ranges" *IEEE Journal of Solid State Circuits*, Vol. 29, No. 1, pp. 46-55, January 1994

[3] S. Otaka, R. Fujimoto and H. Tanimoto, "A 1.9 GHz direct conversion transmitter IC with low power on-chip frequency doubler" *IEICE Trans. Fundamentals*, Vol. E82-A, No. 2, pp. 313-319, February 1999

[4] K. Kimura, H. Asazawa, "Frequency mixer with a frequency doubler for integrated circuits" *IEEE Journal of Solid State Circuits*, Vol. 29, No. 9, pp. 1133-1137, September 1994

[5] B. Gilbert, "The micromixer: A higly linear variant of the gilbert mixer using a bisymmetric class AB input stage" *IEEE Journal of Solid State Circuits*, Vol. 32, No. 9, pp. 1414-1423, September 1997

[6] C. Toumazou, F. J. Lidgey and D. G. Haigh, *Analog IC design: the current-mode approach*, London: IEE, ch. 2, 1990

[7] A. B. Grebene, *Bipolar and MOS analog integrated circuit design*, New York: John Wiley & Sons, Inc., 1984

[8] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *Analysis and design of analog integrated circuits*, Fourth edition, New York: John Wiley & Sons, Inc., 2001

[9] R. W. Rhea, *Oscillator design and computer simulation*, Second edition, New York, McGraw-Hill Companies Inc., 1997